

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

1-11. (Canceled).

12. (Currently Amended) The control unit as recited in Claim ~~[[11]]~~ 16, wherein the at least two clock outputs are connected in such a manner that the control unit generates a monitoring signal as a function of the output signals.

13. (Previously Presented) The control unit as recited in Claim 12, further comprising: an exclusive-OR element to which the output signals are supplied, respectively, wherein the monitoring signal is generated as a function of a signal of the exclusive-OR element.

14. (Currently Amended) The control unit as recited in Claim ~~[[11]]~~ 16, wherein: the at least two clock outputs are connected in such a manner that the output signals are fed back respectively to a first input and a second input of the processor in order for the processor to monitor the output signals and to generate a monitoring signal as a function thereof.

15. (Canceled).

16. (Currently Amended) A ~~[[The]]~~ control unit ~~as recited in Claim 15~~, further comprising:

a processor outputting a clock pulse;

at least one further circuit, wherein:

a clocked data transmission occurs between the processor and the at least one further circuit;

the processor monitors the clock pulse based on output signals of at least two clock outputs; and

the at least two clock outputs are connected in such a manner that the clock pulse is generated as a function of the output signals; and

an OR element to which the at least two clock outputs are supplied to generate the clock pulse.

17. (Currently Amended) The control unit as recited in Claim 16, ~~further comprising~~ wherein:

the OR element comprises:

a first diode; and

a second diode; and ~~, wherein~~

the first diode and the second diode cooperate to perform an OR operation on the at least two clock outputs.

18. (Currently Amended) The control unit as recited in Claim ~~[[11]]~~ 16, wherein the clock pulse is supplied to at least one of an impedance transformer and an amplifier.

19. (Currently Amended) The control unit as recited in Claim ~~[[11]]~~ 16, wherein the at least two clock outputs are assigned to different port groups.

20. (Previously Presented) The control unit as recited in Claim 14, wherein the first input and the second input are assigned to different port groups.